

CLAIMS

What is claimed is:

Sub B. 008260-88942960

1 1. An apparatus, comprising:
2 a metal-oxide-semiconductor transistor with a shifted flat band
3 magnitude;
4 a gate electrode coupled to said metal-oxide-semiconductor
5 transistor and to a positive voltage source; and
6 a source electrode, a drain electrode, and a substrate electrode
7 coupled to each other and to a negative voltage
8 source.

1 2. The apparatus of claim 1, wherein said metal-oxide-
2 semiconductor includes a gate area material with a work function less
3 than - 0.56 volts.

sub A. 1 3. The apparatus of claim 2, wherein said gate area material is
2 platinum silicate.

1 4. The apparatus of claim 2, wherein said gate area material is
2 selected from the group consisting of tantalum nitrate, iridium, nickel,
3 and arsenic.

1 5. The apparatus of claim 1, wherein said metal-oxide-
2 semiconductor transistor includes a heavily-doped substrate area.

1 6. The apparatus of claim 1, wherein said metal-oxide-
2 semiconductor transistor is a p-channel device.

1 7. The apparatus of claim 1, wherein said metal-oxide-
2 transistor is an n-channel device.

1 8. A method, comprising:
2 shifting a flat band magnitude in a metal-oxide-semiconductor
3 transistor;
4 coupling a gate electrode of said metal-oxide-semiconductor
5 transistor to a positive voltage source; and
6 coupling a source electrode, a drain electrode, and a substrate
7 electrode of said metal-oxide-semiconductor
8 transistor to a negative voltage source.

1 9. The method of claim 8, wherein said shifting includes
2 utilizing a gate area with a material whose work function is less than
3 - 0.56 volts.

1 10. The method of claim 9, wherein said material is platinum
2 silicate.

1 11. The method of claim 9, wherein said material is selected
2 from the group consisting of tantalum nitrate, iridium, nickel, and
3 arsenic.

1 12. The method of claim 8, wherein said shifting includes
2 utilizing a substrate which is heavily-doped.

1 13. The method of claim 8, wherein said metal-oxide-
2 semiconductor transistor is a p-channel device.

1 14. The method of claim 8, wherein said metal-oxide-
2 semiconductor transistor is an n-channel device.

15. An apparatus, comprising:
means for shifting a flat band magnitude in a metal-oxide-
semiconductor transistor;
means for coupling a gate electrode of said metal-oxide-
semiconductor transistor to a positive voltage source;
and
means for coupling a source electrode, a drain electrode, and a
substrate electrode of said metal-oxide-
semiconductor transistor to a negative voltage
source.

16. The apparatus of claim 15, wherein said means for shifting
includes a gate area with a material whose work function is less than
- 0.56 volts.

1 17. The apparatus of claim 16, wherein said material is
2 platinum silicate.

1 18. The apparatus of claim 16, wherein said material is
2 selected from the group consisting of tantalum nitrate, iridium, nickel,
3 and arsenic.

1 19. The apparatus of claim 15, wherein said means for shifting
2 includes a substrate which is heavily-doped.

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